芯荣半导体
ChipExtra Semiconductor

# CES34C04A

## 4Kbit Serial I²C bus EEPROM

## DESCRIPTION

The 34C04A(CES34C04A) provides 4096 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 512words of 8 bits each.
The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The 34C04A is accessed via a two-wire serial interface and is available in 1.7V (1.7V to 5.5V) version.

## FEATURES

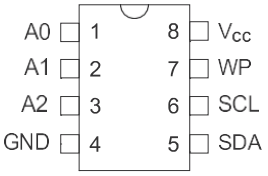
- Wide Voltage Operation $V_{CC}$ = 1.7V to 5.5V
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized: 512 × 8 (4K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz (5V, 3V), 400 KHz (1.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 16-byte Page Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - ➢ Endurance: 1 Million Write Cycles
  - ➢ Data Retention: 100 Years
- PDIP8, SOP8, TSSOP8, UDFN8 Packages

## APPLICATIONS

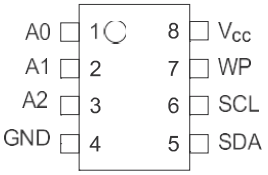
- Intelligent Instrument
- Household Appliance
- Automotive Electronics
- Communications
- consumer electronic

## PIN CONFIGURATION

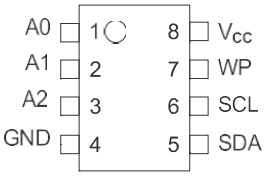
**PDIP8**



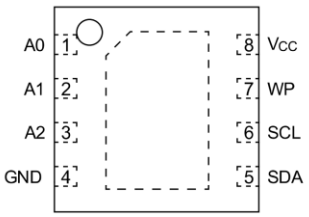

**SOP8**




**TSSOP8**




**UDFN8**



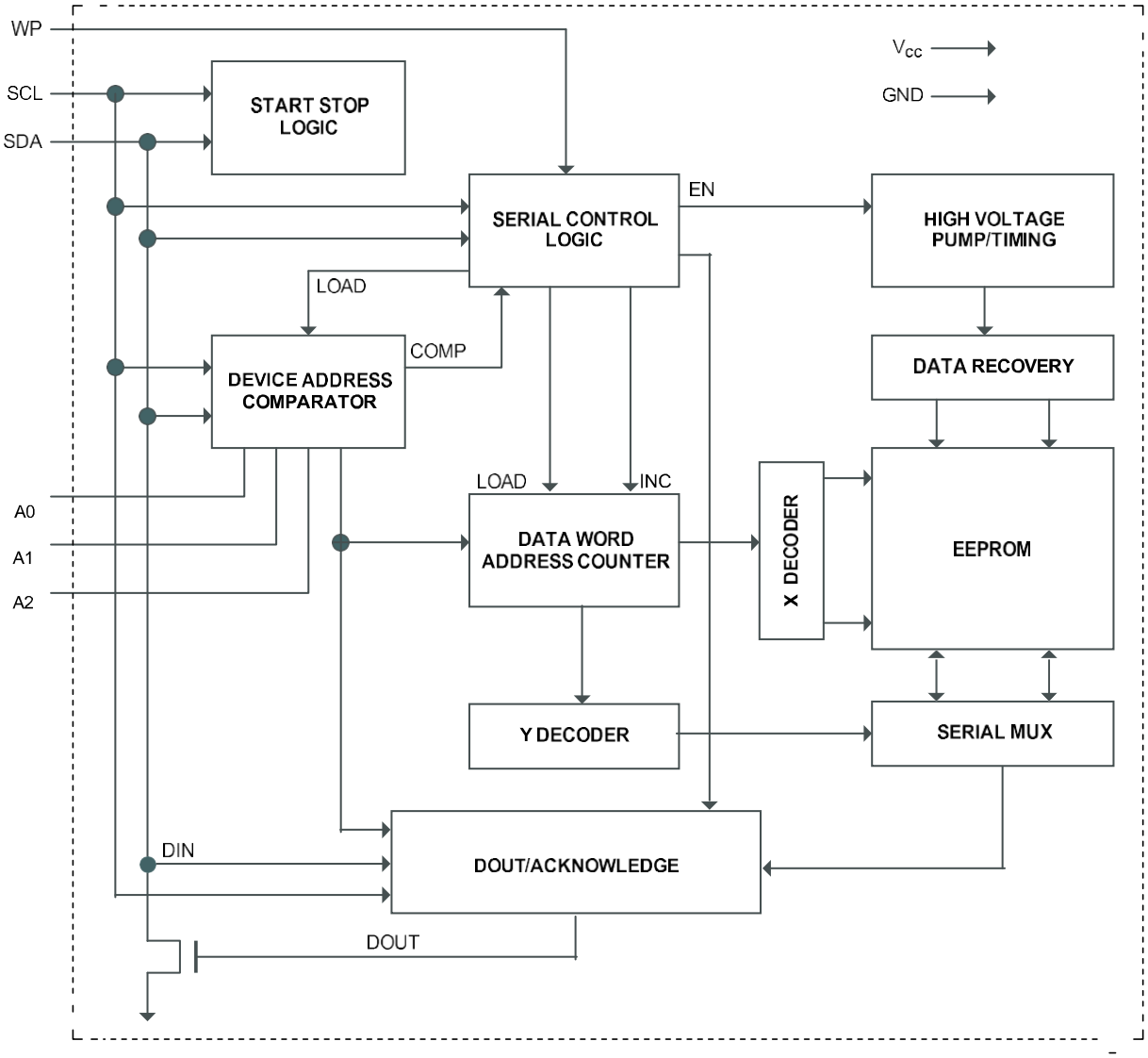

**(Top View)**

## ORDERING INFORMATION

| Temperature Range | Package | | MARK* | Orderable Device | Package Qty. |
|---|---|---|---|---|---|
| -40°C ~ +85°C | Pb-Free | PDIP8 | C34C04A<br>YYWW<br>XX | CES34C04APD8 | 50 Units/Tube |
| | | SOP8 | | CES34C04ASP8 | 4000 Units/R&T |
| | | TSSOP8 | | CES34C04ATSP8 | 4000 Units/R&T |
| | | UDFN8 | | CES34C04AUDN8 | 3000 Units/R&T |

*Note: YYWW---Year&Week; XX----Factory code

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

(Maximum Ratings are those values beyond which damage to the device may occur.)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | -0.3 ~ + 6.5 | V |
| DC Input Voltage | $V_{IN}$ | GND - 0.3 ~ $V_{CC}$ + 0.3 | V |
| DC Output Voltage | $V_{OUT}$ | GND - 0.3 ~ $V_{CC}$ + 0.3 | V |
| Operating Ambient Temperature | $T_a$ | -55 ~ +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

(Functional operation should be restricted to the Recommended Operating Conditions.)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | 1.7 | 5.5 | V |
| Operating Temperature | $T_A$ | -40 | +85 | °C |

## CAPACITANCE

(Applicable over recommended operating range from $T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = +1.7V)

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input/Output Capacitance (SDA) | $C_{I/O}$ | $V_{I/O}$ = 0V | - | 8 | pF |
| Input Capacitance (A0, A1, A2, SCL) | $C_{IN}$ | $V_{IN}$ = 0V | - | 6 | pF |

## DC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from: $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V unless otherwise noted)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | - | | 1.7 | - | 5.5 | V |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 5V | Read at 400kHz | - | 0.4 | 1.0 | mA |
| | | | Write at 400kHz | - | 2.0 | 3.0 | mA |
| Standby Current | $I_{SB}$ | $V_{IN}$ = $V_{CC}$ or GND | | - | - | 3.0 | μA |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{CC}$ or GND | | - | - | 3.0 | μA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{CC}$ or GND | | - | 0.05 | 3.0 | μA |
| Input Low Level | $V_{IL}$ | $V_{CC}$ = 1.8V to 5.5V | | -0.3 | - | $V_{CC}$x0.3 | V |
| | | $V_{CC}$ = 1.7V | | -0.3 | - | $V_{CC}$x0.2 | |
| Input High Level | $V_{IH}$ | $V_{CC}$ = 1.7V to 5.5V | | $V_{CC}$x0.7 | - | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 1.7V | | $V_{CC}$x0.7 | - | $V_{CC}$+0.3 | |
| Output Low Level | $V_{OL3}$ | $I_{OL}$ = 3.0 mA | | - | - | 0.4 | V |
| | $V_{OL2}$ | $I_{OL}$ = 2.1 mA | | - | - | 0.4 | V |
| | $V_{OL1}$ | $I_{OL}$ = 0.15 mA | | - | - | 0.2 | V |

## AC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V, $C_L$ = 1 TTL Gate and 100 pF unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency, SCL | $f_{SCL}$ | 1.7V<$V_{CC}$<2.5V | - | - | 400 | kHz |
| | | 2.5V<$V_{CC}$<5.5V | - | - | 1000 | |
| Clock Pulse Width Low | $t_{LOW}$ | 1.7V<$V_{CC}$<2.5V | 1.2 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.6 | - | - | |
| Clock Pulse Width High | $t_{HIGH}$ | 1.7V<$V_{CC}$<2.5V | 0.6 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.4 | - | - | |
| Noise Suppression Time | $t_I$ | 1.7V<$V_{CC}$<2.5V | - | - | 50 | ns |
| | | 2.5V<$V_{CC}$<5.5V | - | - | 40 | |
| Clock Low to Data Out Valid | $t_{AA}$ | 1.7V<$V_{CC}$<2.5V | 0.05 | - | 0.9 | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.05 | - | 0.55 | |
| Time the bus must be free before a new transmission can start | $t_{BUF}$ | 1.7V<$V_{CC}$<2.5V | 1.2 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.5 | - | - | |
| Start Hold Time | $t_{HD.STA}$ | 1.7V<$V_{CC}$<2.5V | 0.6 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.25 | - | - | |
| Start Setup Time | $t_{SU.STA}$ | 1.7V<$V_{CC}$<2.5V | 0.6 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.25 | - | - | |
| Data In Hold Time | $t_{HD.DAT}$ | 1.7V<$V_{CC}$<5.5V | 0 | - | - | μs |
| Data In Setup Time | $t_{SU.DAT}$ | 1.7V<$V_{CC}$<5.5V | 100 | - | - | ns |
| Inputs Rise Time | $t_R$ | - | - | - | 300 | ns |
| Inputs Fall Time | $t_F$ | 1.7V<$V_{CC}$<2.5V | - | - | 300 | ns |
| | | 2.5V<$V_{CC}$<5.5V | - | - | 100 | |
| Stop Setup Time | $t_{SU.STO}$ | 1.7V<$V_{CC}$<2.5V | 0.6 | - | - | μs |
| | | 2.5V<$V_{CC}$<5.5V | 0.25 | - | - | |
| Data Out Hold Time | $t_{DH}$ | - | 50 | - | - | ns |
| Write Cycle Time | $t_{WR}$ | - | - | 1.5 | 5 | ms |
| 5.0V,25°C,Byte Mode | Endurance | - | 1M | - | - | Write Cycles |

Note:

1. This parameter is characterized and is not 100% tested.
2. AC measurement condition :
   Input pulse voltages: 0.3 $V_{CC}$ to 0.7 $V_{CC}$;
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 $V_{CC}$
   The value of $R_L$ should be concerned according to the actual loading on the user's system.
   $R_L$ (connects to $V_{CC}$): 1.3KΩ （2.5V,5V）, 10KΩ （1.7V）

## PIN DESCRIPTION

| No. | Name | Function Description |
|---|---|---|
| 1 | A0 | Address input.<br>The 34C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 34C04 devices may be addressed on a single bus system. The A0 pin is a no connect and can be connected to ground. |
| 2 | A1 | |
| 3 | A2 | |
| 4 | GND | Circuit ground pin. |
| 5 | SDA | Serial address and data I/O. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices. |
| 6 | SCL | Serial clock input. The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device. |
| 7 | WP | Write protect. The WP pin that provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to $V_{CC}$, the write protection feature is enabled and read only. |
| 8 | VCC | Positive supply voltage. |

## MEMORY ORGANIZATION

| Device | Total bits | Total pages | Bytes per page | Word address |
|---|---|---|---|---|
| 34C04A | 4K | 32 | 16 | 9-bit |

## DEVICE OPERATION

### Clock and data transitions

The device supports the $I^2C$ protocol. This is summarized in Figure 1. Any device that sends data onto the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus master, and the other device is known as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

### Start Conditions

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

### Stop Conditions

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master.

A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

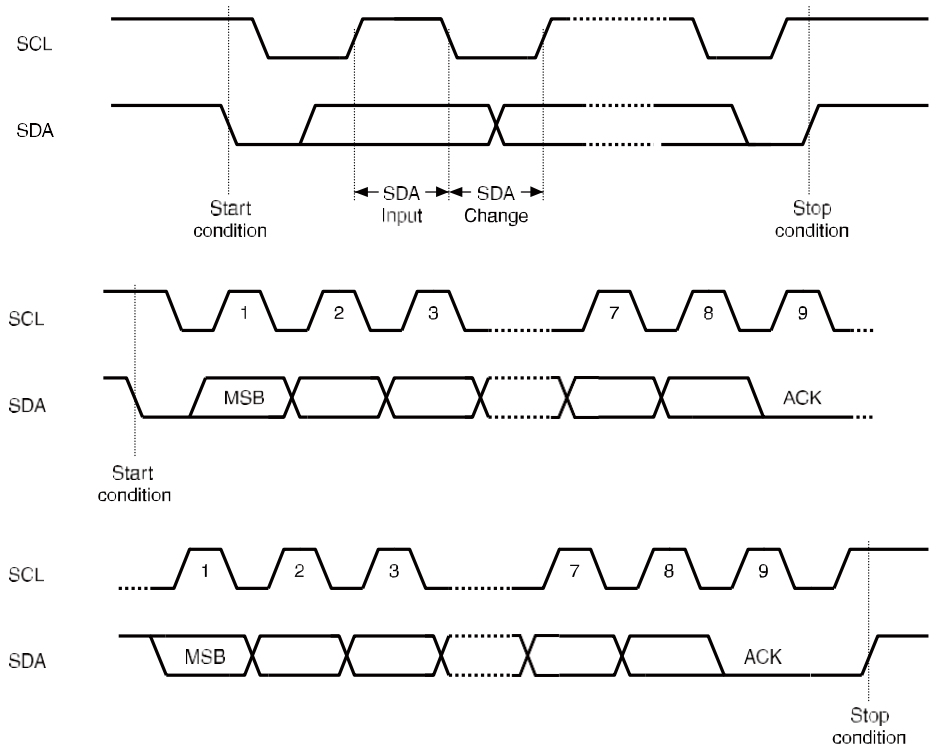



**Figure 1. Bus protocol**

**Acknowledge**

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether a bus master or a slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

**Data Input**

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven low.

**Memory Reset**

To start a communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 1 (on Serial Data (SDA), most significant bit first).

The Device Type Identifier Code (DTIC) consists of a 4-bit device type identifier, and a 3-bit slave address (A2, A1, A0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

**Table 1. Device Type Identifier Code (DTIC)**

| | Abbr | Device type identifier | | | | Select address (2) (3) | | | R_W_n | A0 pin (4) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| Read | RSPD | 1 | 0 | 1 | 0 | LSA2 | LSA1 | LSA0 | 1 | 0 or 1 |
| Write | WSPD | | | | | | | | 0 | |
| Set Write Protection, block 0 | SWP0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | $V_{HV}$ |
| Set Write Protection, block 1 | SWP1 | | | | | 1 | 0 | 0 | 0 | $V_{HV}$ |
| Set Write Protection, block 2 | SWP2 | | | | | 1 | 0 | 1 | 0 | $V_{HV}$ |
| Set Write Protection, block 3 | SWP3 | | | | | 0 | 0 | 0 | 0 | $V_{HV}$ |
| Clear All Write Protection | CWP | | | | | 0 | 1 | 1 | 0 | $V_{HV}$ |
| Read Protection Status, block 0 (5) | RPS0 | | | | | 0 | 0 | 1 | 1 | 0,1,or $V_{HV}$ |
| Read Protection Status, block 1 (5) | RPS1 | | | | | 1 | 0 | 0 | 1 | 0,1,or $V_{HV}$ |
| Read Protection Status, block 2 (5) | RPS2 | | | | | 1 | 0 | 1 | 1 | 0,1,or $V_{HV}$ |
| Read Protection Status, block 3 (5) | RPS3 | | | | | 0 | 0 | 0 | 1 | 0,1,or $V_{HV}$ |
| Set Page Address to 0 (6) | SPA0 | | | | | 1 | 1 | 0 | 0 | 0,1,or $V_{HV}$ |
| Set Page Address to 1 (6)S | SPA1 | | | | | 1 | 1 | 1 | 0 | 0,1,or $V_{HV}$ |
| Read Page Address (7) | RPA | | | | | 1 | 1 | 0 | 1 | 0,1,or $V_{HV}$ |
| Reserved | - | | | | | All other encodings | | | | |

**Note:**

1.The most significant bit, b7, is sent first.

2.Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins.

3.The order of block select bits (b3 and b1) is not a simple binary encoding of the block number.

4.A0 pin is driven to GND, Vcc or VHV.

5.Reading the block protection status results in Ack when the block is not write-protected, and results in NoAck when the block is write-protected.

6.Setting the EE page address to 0 selects the lower 256 bytes of EEPROM; setting it to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.

7.Reading the EE page address results in Ack when the current page is 0, and NoAck when the current page is 1.

Up to eight memory devices can be connected on a single serial bus. Each one is given a unique 3-bit code on the slave address (A2, A1, A0) inputs. When the device select code is received, the device only responds if the slave address is the same as the value on the slave address (A2, A1, A0) inputs.

The 8th bit is the Read/ $\overline{\text{write}}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

## WRITE OPERATIONS

Following a Start condition, the bus master sends a device select code with the RW bit reset to 0. The device acknowledges this, as shown in Figure 2, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10$^{th}$ bit" time slot), either at the end of a Byte write or a Page write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

### Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 2.

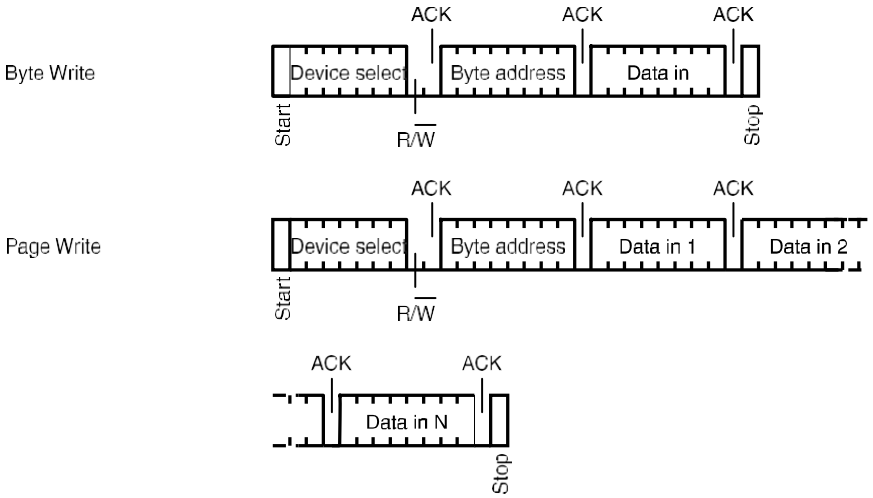



**Figure 2. Write mode sequences in a non write-protected area**

### Page Write

The Page write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control (WP) is low. If the addressed location is hardware write-protected, the device

replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

**Minimizing system delays by polling on ACK**

The sequence, as shown in Figure 3, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

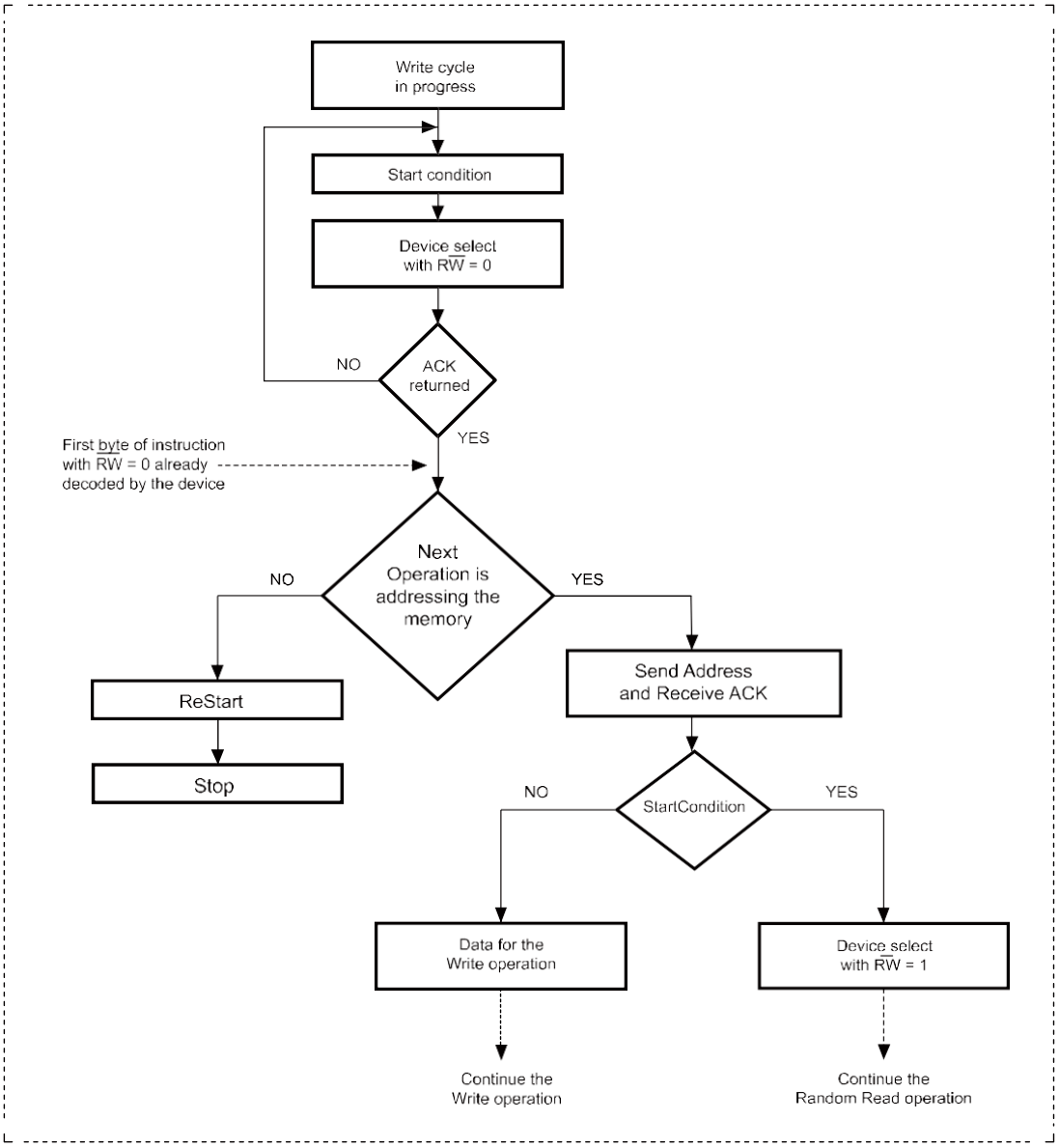



**Figure 3. Write cycle polling flowchart using ACK**

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. To make use of this, a polling sequence can be used by the bus master.

## READ OPERATIONS

Read operations are performed independently of whether a hardware or software protection has been set.The device has an internal address counter which is incremented each time a byte is read.

### Random address read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 4) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

### Current Address Read

For the Current address read operation, following a Start condition, the bus master only sends a device select code with the R $\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 4, without acknowledging the byte.

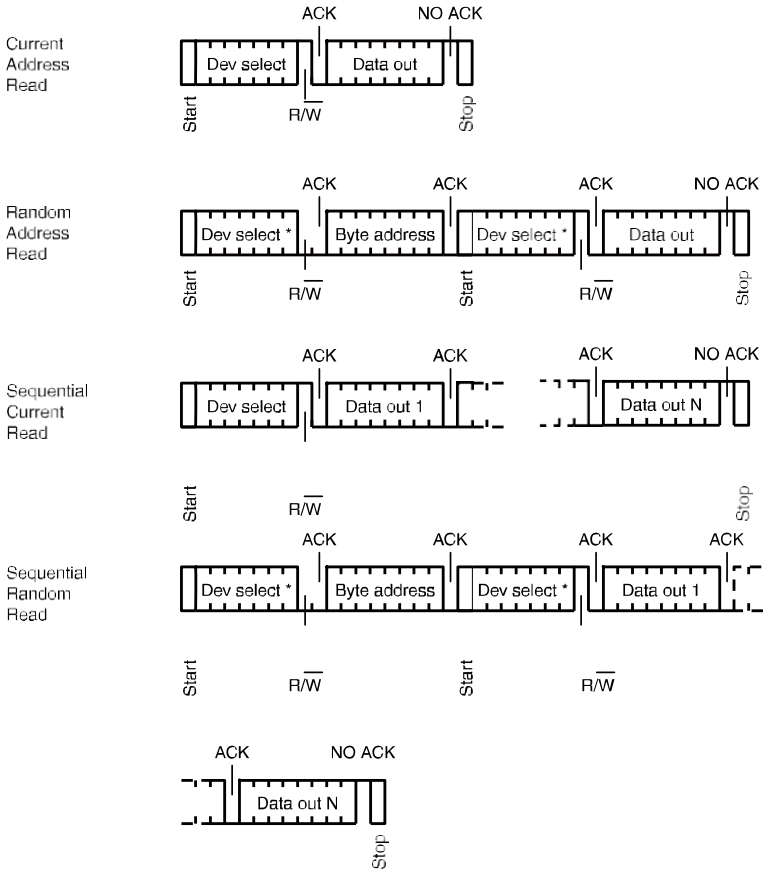



**Figure 4. Read mode sequences**

**Sequential read**

This operation can be used after a Current address read or a Random address read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 4.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

**Acknowledge in read mode**

For all Read commands, after each byte read, the device waits for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

Note: The seven most significant bits of the device select code of a Random Read (in the 1st and 3rd bytes) must be identical.

## SETTING THE WRITE PROTECTION

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 1

The device has three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection status for block n

The level of write protection (set or cleared), that has been defined using these instructions, remains defined even after a power cycle.The DTICs of the SWP, CWP and RPS instructions are defined in Table 1.

**Set and clear the write protection (SWPn and CWP)**

If the software write protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.

When decoded, SWPn and CWPn trigger a write cycle lasting $t_{WR}$.

The DTICs of the SWP and CWP instructions are defined in Table 1.

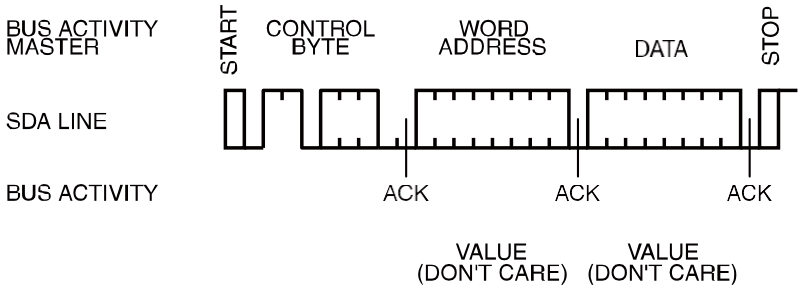



**Figure 5. Setting the write protection**

**Read the protection status (RPSn)**

The serial bus master issues an RPSn command specifying which block to report upon. If the software write protection has not been set, the device replies to the data byte with an Ack. If it has been set, the device replies to the data byte with a NoAck.

The DTIC of the RPSn instruction is defined in Table 1.

**Set the page address (SPAn)**

The SPAn command selects the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the page address is always 0, selecting the lower 256 bytes.

The DTIC of the SPAn instruction is defined in Table 1.

**Read the page address (RPA)**

The RPA command determines if the currently selected page is 0 (device returns Ack) or 1 (device returns NoAck).

The DTIC of the RPA instruction is defined in Table 1.

## INITIAL DELIVERY STATE

The device is delivered with all bits in the memory array set to ‘1’ (each byte contains FFh).

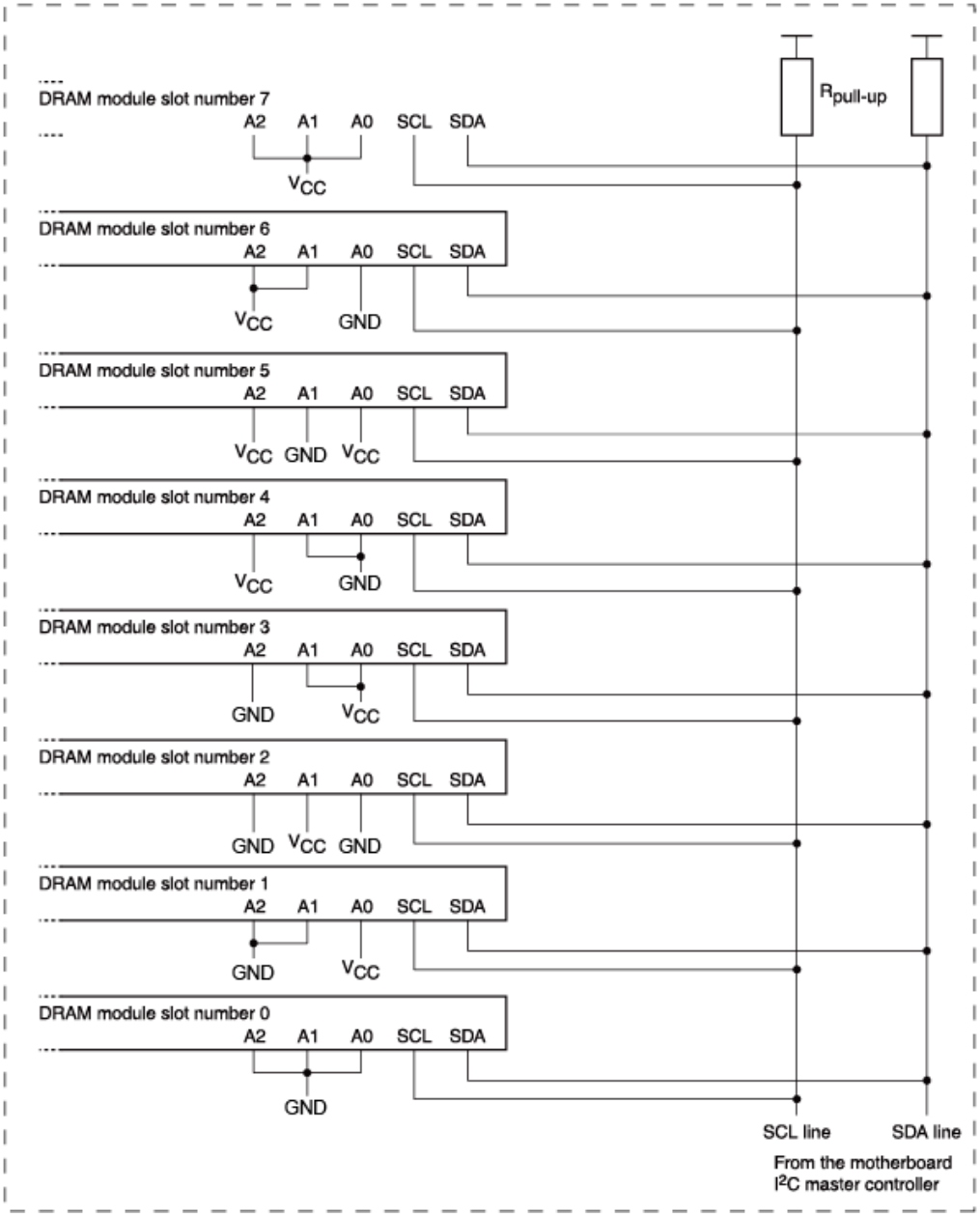
## USE WITHIN A DDR4 DRAM MODULE

In the application, the 34C04A is soldered directly in the printed circuit module. The three slave address inputs (A2, A1, A0) must be connected to GND or $V_{CC}$ directly (that is without using a serial resistor) through the DRAM module connector (see Table 2). The pull-up resistor on SDA is connected on the SMBus of the motherboard (as shown in Figure 6).

The Write Control (WP) of the 34C04A can be left unconnected. However, connecting it to GND is recommended, to maintain full read and write access.

**Table 2. DRAM DIMM connections**

| DIMM position | A2 | A1 | A0 |
|---|---|---|---|
| 0 | GND | GND | GND |
| 1 | GND | GND | $V_{CC}$ |
| 2 | GND | $V_{CC}$ | GND |
| 3 | GND | $V_{CC}$ | $V_{CC}$ |
| 4 | $V_{CC}$ | GND | GND |
| 5 | $V_{CC}$ | GND | $V_{CC}$ |
| 6 | $V_{CC}$ | $V_{CC}$ | GND |
| 7 | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |




1.A0, A1 and A2 are wired at each DRAM module slot in a binary sequence for a maximum of 8 devices.

2.Common clock and common data are shared across all the devices.

**Figure 6. Serial presence detect block diagram**

## PROGRAMMING THE 34C04

The situations in which the M34E04 is programmed can be considered under two headings:
- when the DDR4 DRAM is isolated (not inserted on the PCB motherboard)
- when the DDR4 DRAM is inserted on the PCB motherboard

### Isolated DRAM module

With a specific programming equipment, it is possible to define the M34E04 content, using Byte and Page write instructions, and the write-protection SWP(n) and CWP instructions. To issue the SWP(n) and CWP instructions, the signal applied on SA0 must be driven to $V_{HV}$ during the whole instruction.

### DRAM module inserted in the application motherboard

Table 3 and Table 4 show how the Ack bits can be used to identify the write-protection status.

**Table 3. Acknowledge when writing data or defining the write-protection status (instructions with R/W bit = 0)**

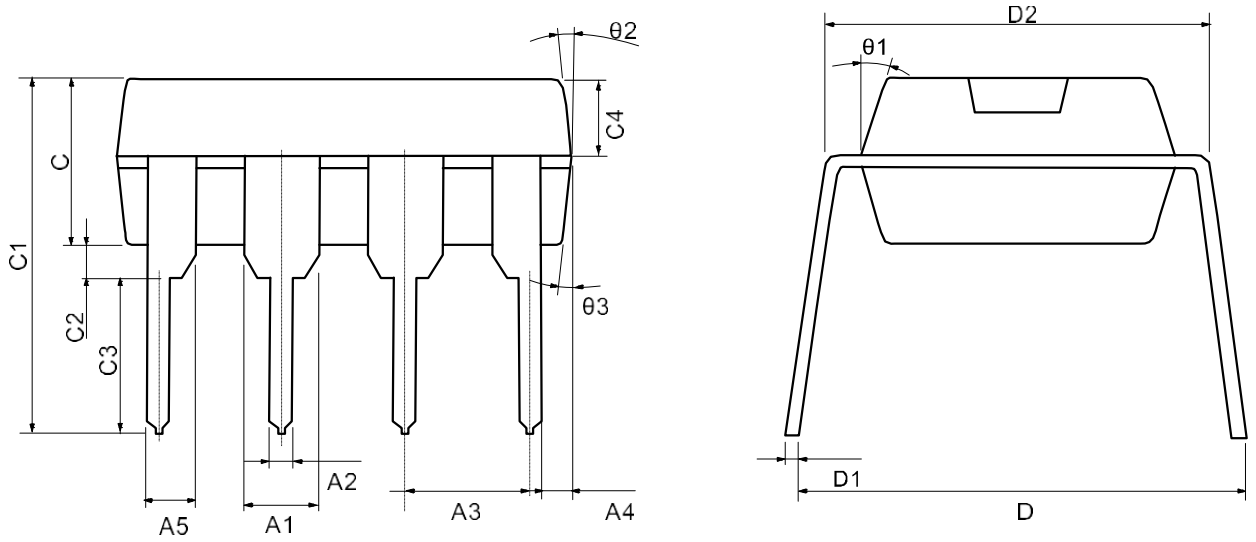
| Status | Instruction | Ack | Address | Ack | Data byte | Ack | Write cycle ($t_W$) |
|---|---|---|---|---|---|---|---|
| Protected | SWPn | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | Page or byte write in protected block | Ack | Address | Ack | Data | NoAck | No |
| Not Protected | SWPn or CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | Page or byte write | Ack | Address | Ack | Data | Ack | Yes |

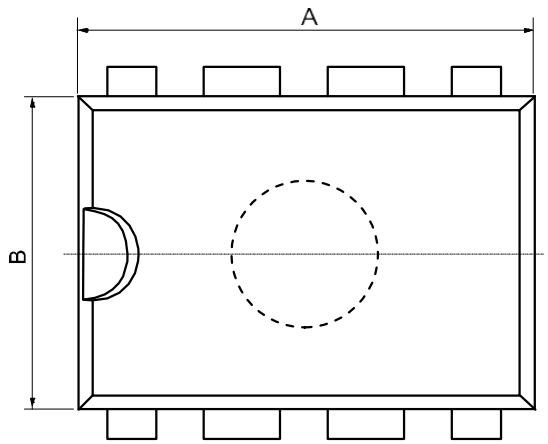
**Table 4. Acknowledge when reading the protection status (instructions with R/W bit = 1)**

| SWPn Status | Instruction | Ack | Address | Ack | Data byte | Ack |
|---|---|---|---|---|---|---|
| Set | RPSn | NoAck | Not significant | NoAck | Not significant | NoAck |
| Not set | RPSn | Ack | Not significant | NoAck | Not significant | NoAck |

## PHYSICAL DIMENSIONS

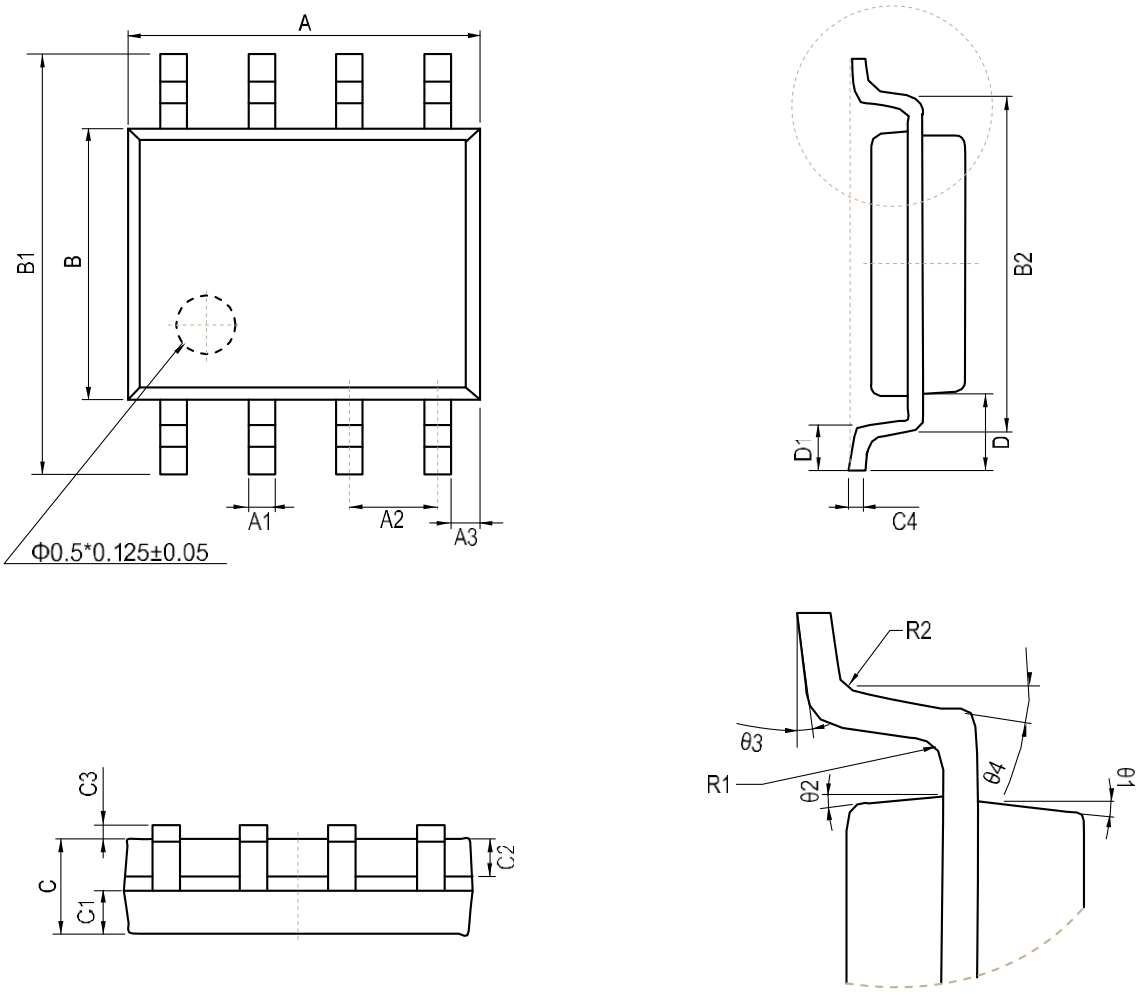
**DIP8**



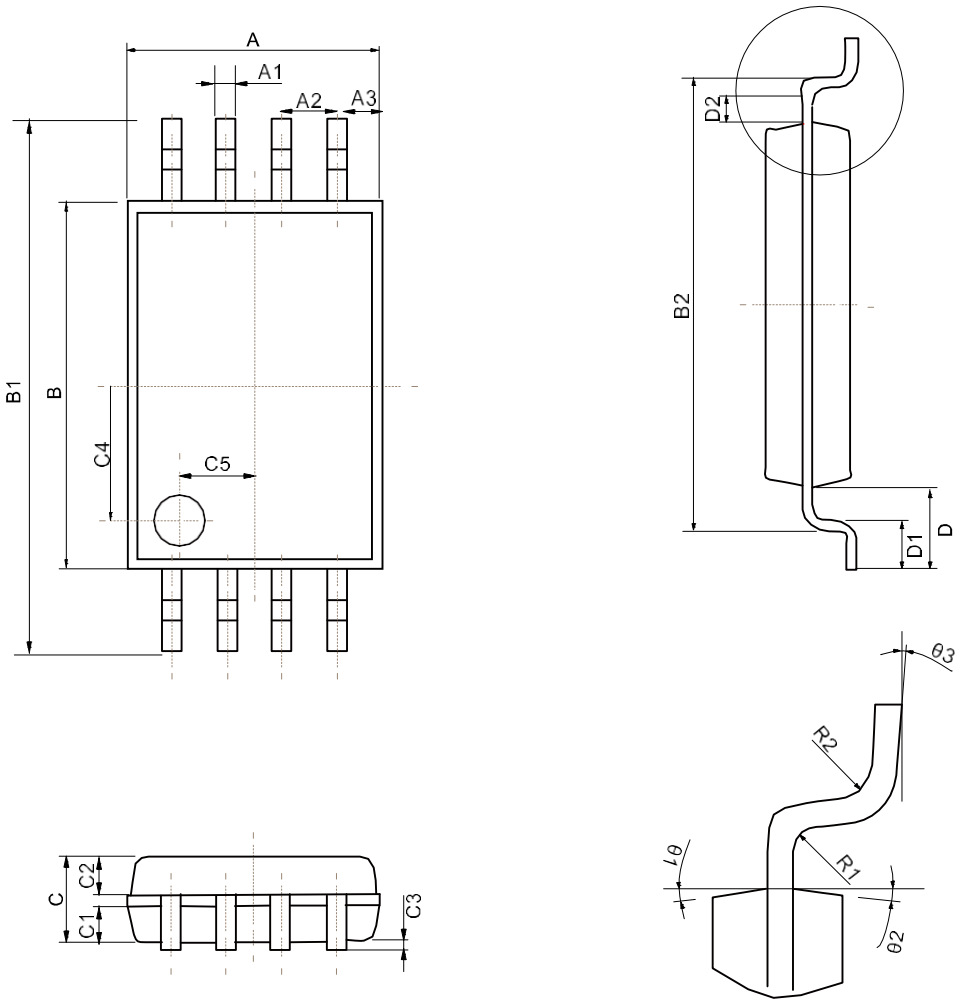

| Symbol | Dimension（mm） | | Symbol | Dimension（mm） | |
|---|---|---|---|---|---|
| | Min | Max | | Min | Max |
| A | 9.00 | 9.20 | C2 | 0.50（TYP） | |
| A1 | 1.474 | 1.574 | C3 | 3.20 | 3.40 |
| A2 | 0.41 | 0.51 | C4 | 1.47 | 1.57 |
| A3 | 2.44 | 2.64 | D | 8.20 | 8.80 |
| A4 | 0.51（TYP） | | D1 | 0.244 | 0.264 |
| A5 | 0.99（TYP） | | D2 | 7.62 | 7.87 |
| B | 6.10 | 6.30 | θ1 | 17°（TYP） | |
| C | 3.20 | 3.40 | θ2 | 10°（TYP） | |
| C1 | 7.10 | 7.30 | θ3 | 8°（TYP） | |

**SOP8**




| Symbol | Dimension（mm） | | Symbol | Dimension（mm） | |
|---|---|---|---|---|---|
| | Min | Max | | Min | Max |
| A | 4.80 | 5.00 | C3 | 0.05 | 0.20 |
| A1 | 0.356 | 0.456 | C4 | 0.203 | 0.233 |
| A2 | 1.27（TYP） | | D | 1.05（TYP） | |
| A3 | 0.345（TYP） | | D1 | 0.40 | 0.80 |
| B | 3.80 | 4.00 | R1 | 0.20（TYP） | |
| B1 | 5.80 | 6.20 | R2 | 0.20（TYP） | |
| B2 | 5.00（TYP） | | θ1 | 17°（TYP） | |
| C | 1.30 | 1.60 | θ2 | 13°（TYP） | |
| C1 | 0.55 | 0.65 | θ3 | 0° ~ 8°（TYP） | |
| C2 | 0.55 | 0.65 | θ4 | 4° ~ 12°（TYP） | |

**TSSOP8**




| Symbol | Dimension（mm） | | Symbol | Dimension（mm） | |
|---|---|---|---|---|---|
| | Min | Max | | Min | Max |
| A | 2.90 | 3.10 | C4 | 1.55 | 1.65 |
| A1 | 0.20 | 0.30 | C5 | 0.85 | 0.95 |
| A2 | 0.60 | 0.70 | D | 1.00（TYP） | |
| A3 | 0.41 | 0.42 | D1 | 0.50 | 0.70 |
| B | 4.30 | 4.50 | D2 | 0.19 | 0.29 |
| B1 | 6.30 | 6.50 | R1 | 0.15（TYP） | |
| B2 | 5.404 | 5.504 | R2 | 0.15（TYP） | |
| C | 0.95 | 1.05 | θ1 | 12°（TYP） | |
| C1 | 0.415 | 0.465 | θ2 | 12°（TYP） | |
| C2 | 0.39 | 0.49 | θ3 | 0° ~ 7° | |
| C3 | 0.05 | 0.15 | - | - | |