芯荣半导体
ChipExtra Semiconductor

CES24C64

64K bit Serial I℃ bus EEPROM 4 ball CSP

Descriptions

The 24C64 provides 65536 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 8192 words of 8 bits each.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The 24C64 is accessed via a two-wire serial interface and is available in 1.7V (1.7V to 5.5V) version.

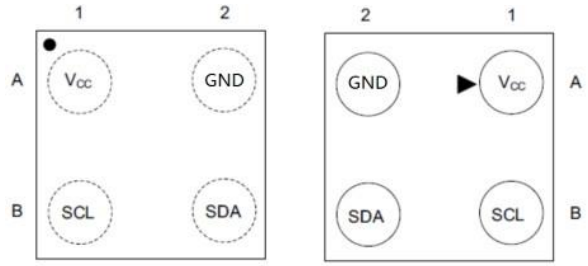
Features

- Wide Voltage Operation VCC = 1.7V to 5.5V
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized:24C64, 8192 × 8 (64K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Page Write, 32-byte Page
- Partial Page Writes Allowed
- Software Write protect
  - Upper quarter memory array
  - Upper half memory array
  - Upper 3/4 memory array
  - Whole memory array
- Configurable device address
- Self-timed Write Cycle (4 ms max)
- High-reliability
- Endurance: 1 Million Write Cycles
- Data Retention: 100 Years
- WLCSP

Typical Application

- Intelligent Instrument
- Camera
- Automotive Electronics
- Wearable Devices

Package Information



Top view **Bottom View**

IC size : 0.67 (W) X 0.67(L) X 0.30(T) (mm)

Minimum pin pitch = 0.4mm (4pins WLCSP)

Ordering Information

PART NUMBER	TEMPERRATURE RANGE	PACKAGE	PINS	SPQ	PACKING
CES24C64CS4	-40 ℃ ~ +85 ℃	WLCSP	4	3000	TAPE & REEL

Pin Description

PIN No.	Pin Name	I/O	Description
1	VCC	P	Power supply
2	SCL	I	I2C interface input/output (CLOCK)
3	SDA	I/O	I2C interface input (DATA), open-drain
4	GND	-	Ground

ABSOLUTE MAXIMUM RATINGS

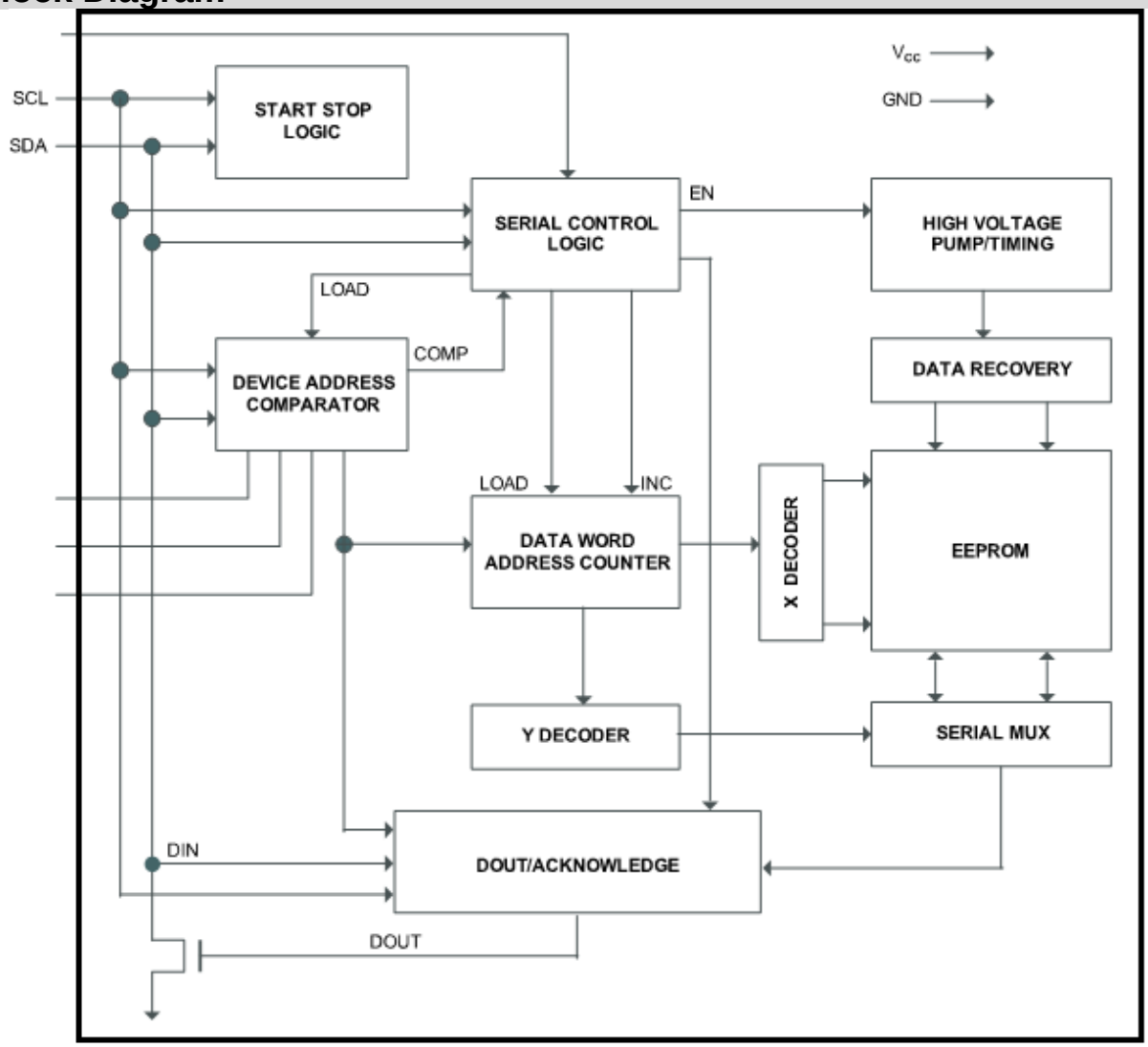
(Maximum Ratings are those values beyond which damage to the device may occur.)

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.3 to + 6.5	V
DC Input Voltage	V_{IN}	GND - 0.3 to V_{CC} + 0.3	V
DC Output Voltage	V_{OUT}	GND - 0.3 to V_{CC} + 0.3	V
Operating Ambient Temperature	Ta	-55 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note:

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range(Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode when the absolute maximum ratings may be exceeded is anticipated.

Block Diagram



Recommended Operating condition

(Functional operation should be restricted to the Recommended Operating Conditions.)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	1.7	5.5	V
Operating Temperature	T_A	-40	+85	°C

Electrical Specification

(Vcc=5.5V, Ta= -40 to 85℃, unless otherwise specified. Typical values are at 25℃)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage	V_{CC1}	-		1.7	-	5.5	V
	V_{CC2}	-		2.5	-	5.5	
	V_{CC3}	-		2.7	-	5.5	
	V_{CC4}	-		4.5	-	5.5	
Supply Current	I_{CC}	V_{CC} = 5V	Read at 400kHz	-		2.0	mA
			Write at 400kHz	-		2.0	mA
Standby Current	I_{SB}	V_{IN} = V_{CC} or GND, V_{CC}=1.7V		-		1.0	μA
		V_{IN} = V_{CC} or GND, V_{CC}=2.5V				2.0	μA
		V_{IN} = V_{CC} or GND, V_{CC}=5.5V		-		2.0	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND		-	0.10	2.0	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or GND		-	0.05	2.0	μA
Input Low Level	V_{IL}	V_{CC} = 1.8V to 5.5V		-0.3	-	0.3 x V_{CC}	V
		V_{CC} = 1.7V		-0.3	-	0.2 x V_{CC}	
Input High Level	V_{IH}	V_{CC} = 1.7V to 5.5V		0.7xV_{CC}	-	V_{CC}+0.3	V
Output Low Level	V_{OL3}	V_{CC} = 5.0V, I_{OL} = 3.0 mA		-	-	0.4	V
	V_{OL2}	V_{CC} = 3.0V, I_{OL} = 2.1 mA		-	-	0.4	V
	V_{OL1}	V_{CC} = 1.7V, I_{OL} = 0.15 mA		-	-	0.2	V

ACELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from T_A = -40℃ to +85℃, V_{CC} = +1.7V to+5.5V, C_L = 1 TTL Gate and 100 pF unless otherwise noted)

Parameter	Symbol	Test	Min	Typ	Max	Unit
Clock Frequency, SCL	f_{SCL}	1.7V<V_{CC}<2.5V	-	-	400	kHz
		2.5V<V_{CC}<5.5V	-	-	1000	
Clock Pulse Width Low	t_{LOW}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.6	-	-	
Clock Pulse Width High	t_{HIGH}	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.4	-	-	
Noise Suppression Time	t_I	1.7V<V_{CC}<2.5V	-	-	50	ns
		2.5V<V_{CC}<5.5V			50	
Clock Low to Data Out Valid	t_{AA}	1.7V<V_{CC}<2.5V	0.1	-	0.9	μs
		2.5V<V_{CC}<5.5V	0.05	-	0.9	
Time the bus must be free before a new transmission can start	t_{BUF}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.5	-	-	
Start Hold Time	$t_{HD.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25			
Data In Hold Time	$t_{HD.DAT}$	1.7V<V_{CC}<5.5V	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	1.7V<V_{CC}<5.5V	100	-	-	ns
Inputs Rise Time	t_R	-	-	-	300	ns
Inputs Fall Time	t_F	-	-	-	300	Ns
Stop Setup Time	$t_{SU.STO}$	1.7V<V_{CC}<2.5V	0.6	-	-	Ms
		2.5V<V_{CC}<5.5V	0.25	-	-	
Data Out Hold Time	t_{DH}	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	-	3.3	4	ms
5.0V,25°C,Byte Mode	Endurance	-	1M	-	-	Write Cycles

Note:

1. This parameter is characterized and is not 100% tested.
2. AC measurement condition :
   (1) Input pulse voltages: 0.3 VCC to 0.7 VCC; Input rise and fall time: 50 ns;
   (2) Input and output timing reference voltages: 0.5 VCC;
   (3) The value of RL should be concerned according to the actual loading on the user’s system;
   (4)RL (connects to VCC): 1.3KΩ（2.5V,5V）, 10KΩ（1.7V）.

MEMORY ORGANIZATION

Device	Total bits	Total pages	Bytes per page	Word address
CES24C64	64K	256	32	13-bit

DEVICE OPERATION

Clock and data transitions

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

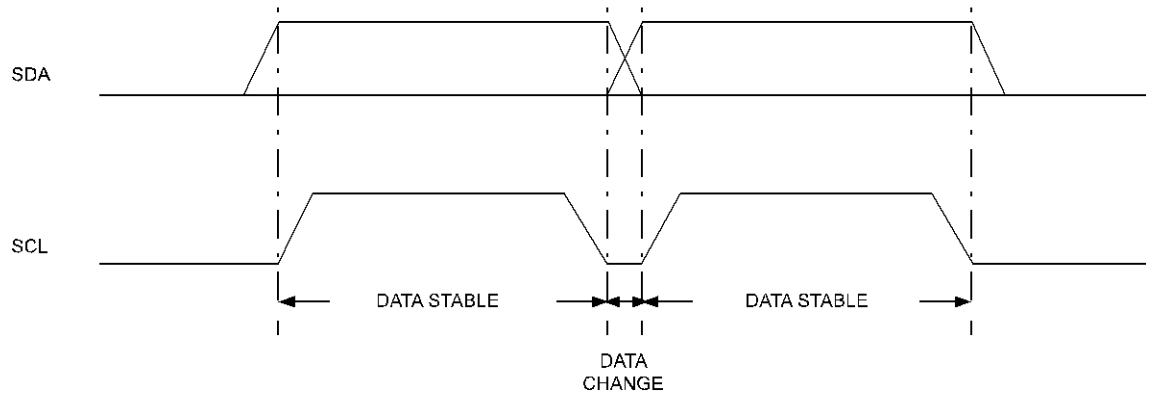


Figure 1. Data Validity

Start Conditions

A high-to-low transition of SDA with SCL high is a start condition which must precede any other Command. (see Figure 2)

Stop Conditions

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode. (see Figure 2)

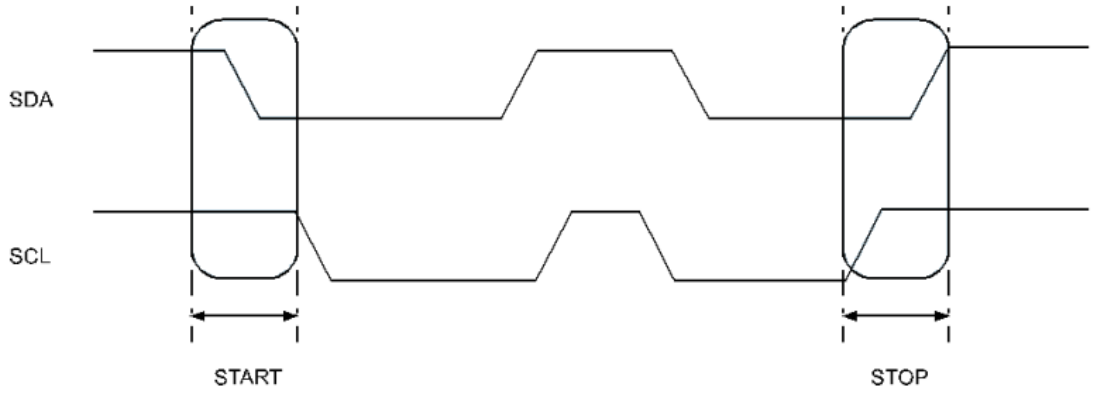


Figure 2. Start and Stop Definition

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode

The EEPROM features a low-power standby mode which is enabled:
(1) upon power-up and (2) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:
(1) Clock up to 9 cycles.
(2) Look for SDA high in each cycle while SCL is high.
(3) Create a start condition.

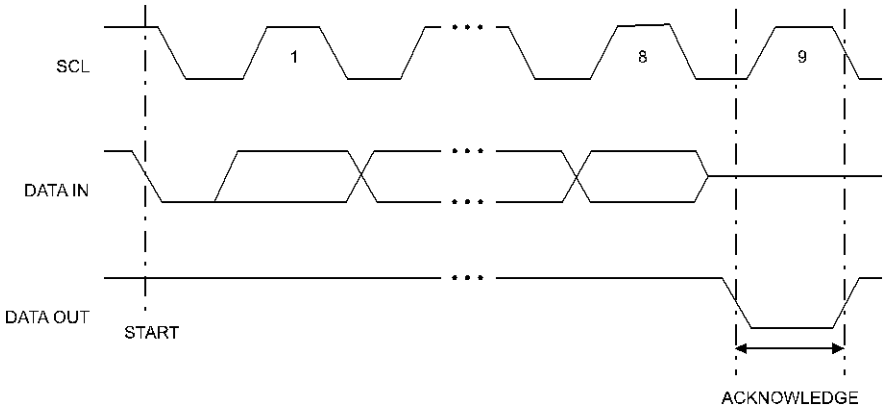


Figure 3. Output Acknowledge

CONFIGURABLE DEVICE ADDRESS(CDA)

Since there are no A0,A1,A2 pins, the 24C64 WLCSP package provides the address configuration for user to implement CDA features. When power-on, the device will load address configuration automatically.

The CDA contains C0/C1/C2 three NVM bits, and corresponding to A0/A1/A2 pins respectively. The CDA factory default is “000”.

Access to this memory location is obtained by beginning the device address word with a “1010” sequence, the behavior of next three bits (C2, C1 and C0) remains the same as during a standard memory addressing sequence(refer to Figure 4).

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

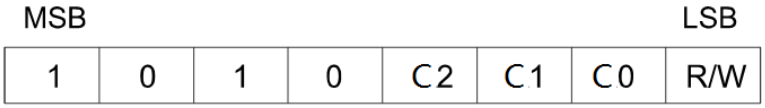


Figure 4. Device Address

WRITE OPERATIONS

Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

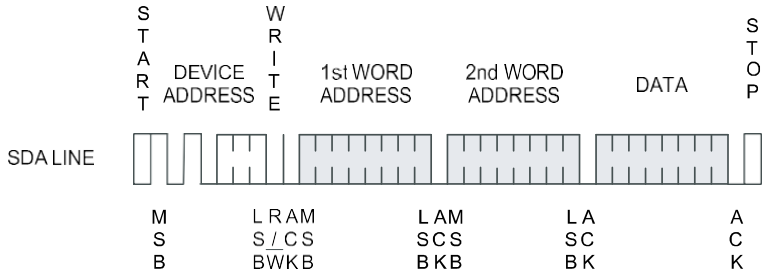


Figure 5. Byte Write

Page Write

The 24C64 devices is capable of 32-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stopcondition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to31more data words. TheEEPROM will respond with a "0" after each data word received. The microcontroller mustterminate the page write sequence with a stop condition (see Figure6).

The data word address lower 5 (24C64) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

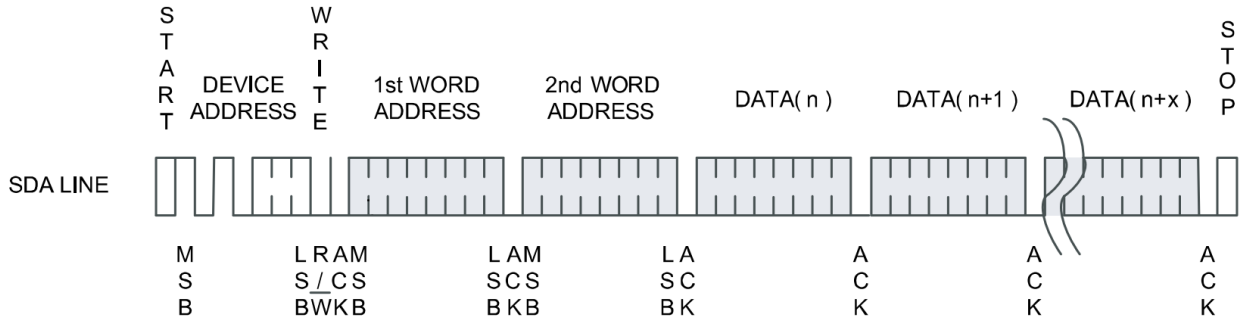


Figure 6. Page Write

Write protection

By writing specific values in a register (Table 5) located at address 1xxx.xxxx.xxxx.xxxxb, the memory array can be write-protected by blocks, which size can be defined as:

- the upper quarter memory array
- the upper half memory array
- the upper 3/4 memory array
- the whole memory array

Table 5. Write Protect register (Address = 1xxx.xxxx.xxxx.xxxxb)

	b7	b6	b5	b4	b3	b2	b1	b0
Write	x	x	x	x	Write protect activation	Size of write protected block	Size of write protected block	x
Read	0	0	0	0				

Note: *Location 1xxx.xxxx.xxxx.xxxxb is outside of the addressing field of the EEPROM memory (16 Kbytes are addressed within the 00xx.xxxx.xxxx.xxxx range)*

(1) Bit b3 enables or disables the Write protection
- b3=0: the whole memory can be written (no Write protection)
- b3=1: the concerned block is write-protected

(2) Bits b2 and b1 define the size of the memory block to be protected against write instructions:
- b2,b1=0,0: the upper quarter of memory is write-protected
- b2,b1=0,1: the upper half memory is write-protected
- b2,b1=1,0: the upper 3/4 of memory are write-protected
- b2,b1=1,1: the whole memory is write-protected

(3) b7, b6, b5, b4,b0 bits are Don't Care bits.

(4) Writing the Write Protect register

Writing in the Write protect register is performed with a Byte Write instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7,b6,b5,b4,b0 of the data byte are not significant (Don't Care). Writing more than one byte will discard the write cycle (Write protect register content will not be changed).

Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue

READ OPERATIONS

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

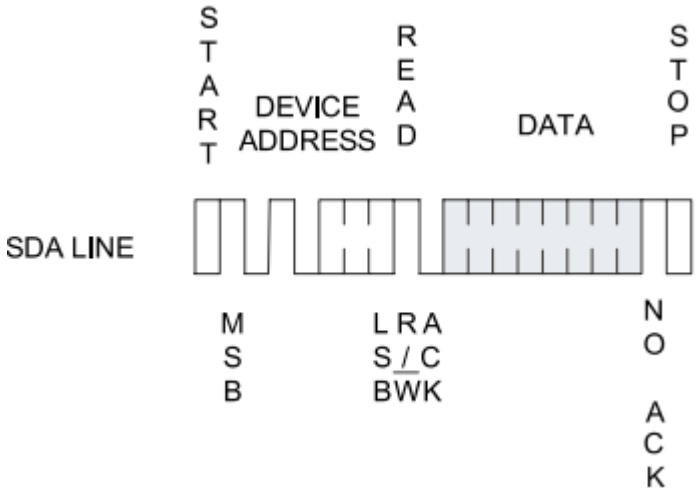


Figure 7. Current Address Read

Radom Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition

(see Figure 8).

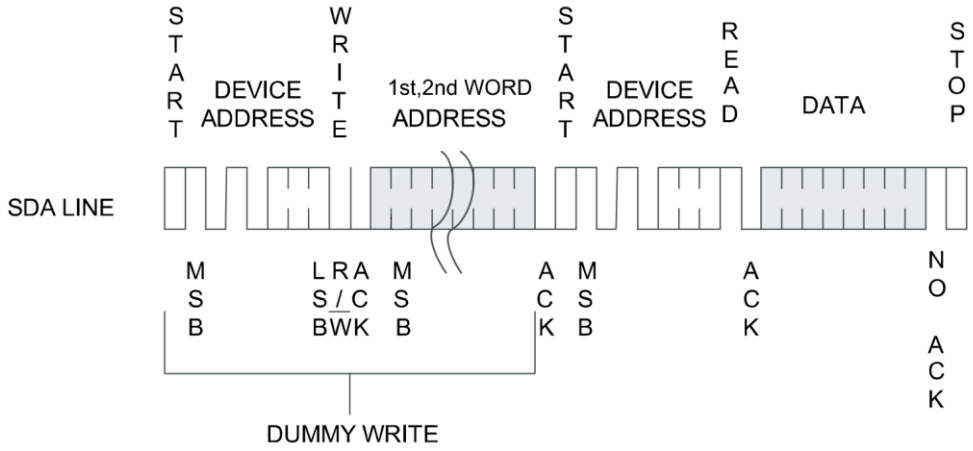


Figure 8. Random Read

Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

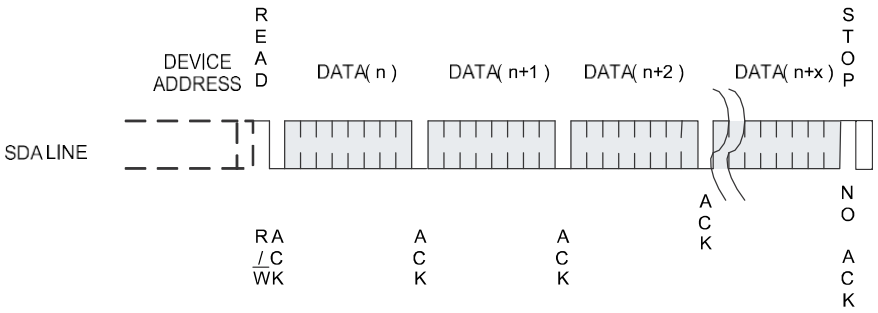


Figure 9. Sequential Read

BUS TIMING

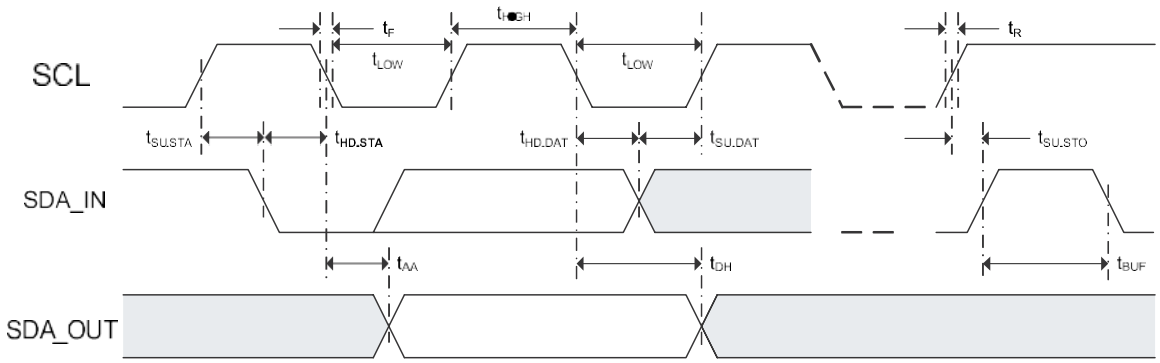


Figure 10. SCL: Serial Clock, SDA: Serial Data

WRITE CYCLE TIMING

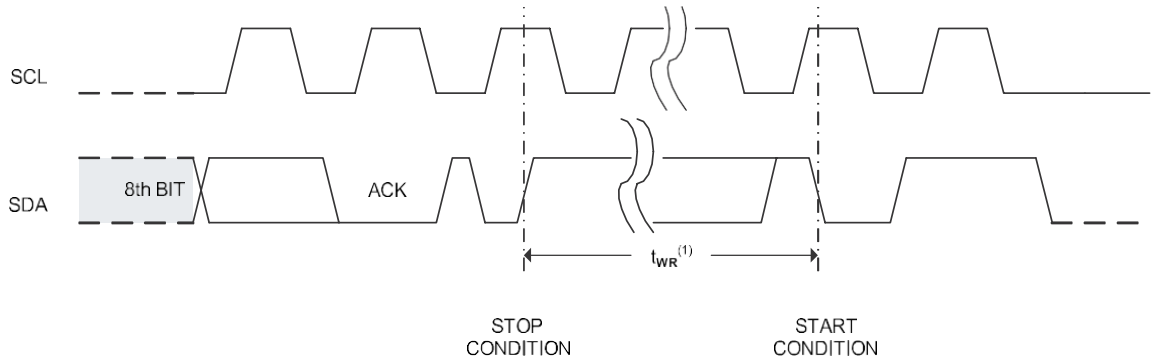
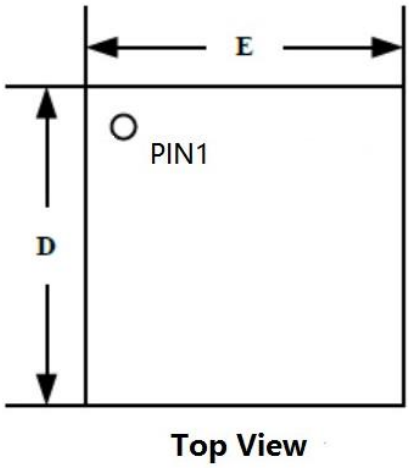


Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

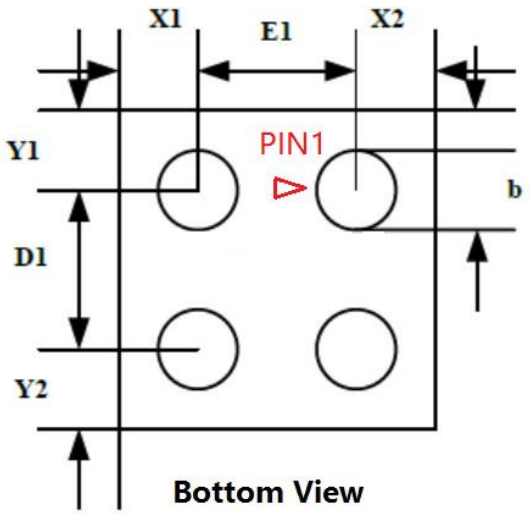
Notes: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

PHYSICAL DIMENSIONS

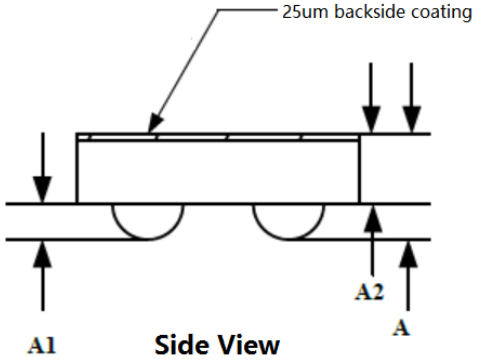
WLCSP-4



Top View



Bottom View



Side View

Unit: mm

Symbol	Min	Typ	Max
A	0.240	0.260	0.280
A1	0.045	0.055	0.065
A2	0.185	0.205	0.225
D	0.624	0.689	0.674
D1		0.400	
E	0.610	0.675	0.660
E1		0.400	
b	0.130	0.160	0.190
X1		137.5	
X2		137.5	
Y1		144.5	
Y2		144.5	